



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: SAKIYAMA ET AL.

Examiner: C. EVERHART

Serial No.: 09/700,940

Group Art Unit: 2825

Filed: NOVEMBER 21, 2000

Docket: 10873.589USWO

Confirmation No.: 4531

No.:

Due Date: MAY 24, 2002

Title: METHOD OF DISPOSING LSI

CERTIFICATE UNDER 37 CFR 1.10

'Express Mail' mailing label number: EV 077890674 US

Date of Deposit: May 24, 2002

I hereby certify that this paper or fee is being deposited with the United States Postal Service 'Express Mail Post Office To Addressee' service under 37 CFR 1.10 and is addressed to the Commissioner for Patents, Washington, D.C. 20231.

By: 

Name: John Junker

Commissioner for Patents
Washington, D.C. 20231

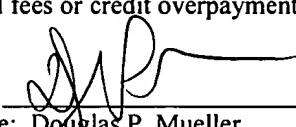
Sir:

We are transmitting herewith the attached:

- ☒ Transmittal Sheet in duplicate containing Certificate of Mailing
- ☒ Amendment Including Version With Markings To Show Changes Made
- ☒ Revised Drawing
- ☒ Request for Extension of Time for 1 month(s) and fee of \$110.00
- ☒ Return postcard

Please consider this a PETITION FOR EXTENSION OF TIME for a sufficient number of months to enter these papers or any future reply, if appropriate. Please charge any additional fees or credit overpayment to Deposit Account No. 13-2725. A duplicate of this sheet is enclosed.

MERCHANT & GOULD P.C.
P.O. Box 2903, Minneapolis, MN 55402-0903
612.332.5300

By: 
Name: Douglas P. Mueller
Reg. No.: 30,300



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By: *John Junkers*
Name: John Junkers

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Amendment

Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

In Response to the Office Action of January 24, 2002, please amend this application as follows:

In The Claims

Please amend claims 1 and 4 as shown below:

- Sub B1*
1. (Once Amended) A LSI layout method for a LSI design by automatic arrangement wiring of standard cells, wherein logic gate cells and power supply capacitor cells are provided as the standard cells, comprising the operations of:
 - determining a capacitance value of the power supply capacitor cells so as to correspond to a drive load capacity value of the logic gate cells,
 - connecting the power supply line of the logic gate with the ground line of the logic gate through the power supply capacitor cells, and
 - arranging the power supply capacitor cells in the vicinity of the logic gate cells.